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Frasier Online Episode Guide: Episode 11.05 - The Placeholder

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1 [Computational models as a vehicle for theoretical linguistics: A computational account of some constraints on language](#)

Mitchell Marcus

 July 1978 **Proceedings of the 1978 workshop on Theoretical issues in natural language processing**

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2 [A computational account of some constraints on language](#)

Mitchell Marcus

 July 1978 **Proceedings of the theoretical issues in natural language processing-2**

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This paper will outline two arguments presented at length in [Marcus 77] demonstrating that important subcases of two of these constraints, the Subjacency Principle and the Specified Subject Constraint, fall out naturally from the 'structure of a grammar interpreter called PARSIFAL, whose structure is in turn based upon the hypothesis that natural language parser needn't simulate a nondeterministic machine. This "Determinism Hypothesis" claims that natural language can be parsed ...

3 [Measurement: A high-level programming environment for packet trace anonymization and transformation](#)

Ruoming Pang, Vern Paxson

 August 2003 **Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications**

Full text available:

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Packet traces of operational Internet traffic are invaluable to network research, but public sharing of such traces is severely limited by the need to first remove all sensitive information. Current trace anonymization technology leaves only the packet headers intact, completely stripping the contents; to our knowledge, there are no publicly available traces of any significant size that contain packet payloads. We describe a new approach to transform and anonymize packet traces. Our tool provide ...

Keywords: anonymization, internet, measurement, network intrusion detection, packet trace, privacy, transformation



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Relevance scale ☐ ☐ ☐ ☐ ☐1 [Constructing instruction traces from cache-filtered address traces \(CITCAT\)](#)

Charlton D. Rose, J. Kelly Flanagan

December 1996 **ACM SIGARCH Computer Architecture News**, Volume 24 Issue 5Full text available: [pdf\(595.54 KB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

Instruction traces are useful tools for studying many aspects of computer systems, but they are difficult to gather without perturbing the systems being traced. In the past, researchers have collected instruction traces through various techniques, including single-stepping, instruction inlining, hardware monitoring, and processor simulation. These approaches, however, fail to produce accurate traces because they interfere with the processor's normal execution. Because processors are deterministic ...

2 [Enhanced visibility and performance in functional verification by reconstruction](#)

Joshua Marantz

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**Full text available: [pdf\(174.85 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)
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Cycle simulators, in-circuit emulators, and hardware accelerators have made it possible to rapidly model the functionality of large digital designs. But these techniques provide limited visibility of internal design nodes, making debugging hard. Simulators run slowly when all nodes are traced. Emulators provide full visibility only with limited depth, or with greatly reduced speed. This paper discusses software techniques for increasing design visibility while reducing tracing overhead in s ...

Keywords: emulation, functional simulation, reconstruction, visibility3 [Preprototyping SIMD coprocessors using virtual machine emulation and trace compilation](#)

Martin C. Herbordt, Owais Kidwai, Charles C. Weems

June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 25 Issue 1Full text available: [pdf\(2.05 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The use of massively parallel SIMD array architectures is proliferating in the area of domain specific coprocessors. Even so, they have undergone few systematic empirical studies. The underlying problems include the size of the architecture space, the lack of portability of the test programs, and the inherent complexity of simulating up to hundreds of thousands of processing elements. We address the computational cost problem with a novel approach to